IPC-A-610E Comments
September 2007

Commenter name, company	Ref	Type	1.	Recommendation	Reason for Recommendation	Committee Resolution
Leo Lambert, EPTAC	Index	E	2.	Add Tinning reference to Index, 6-1, 6-11, 6-12	Clarify and ease of finding.	
Staff	1.4.2		3.	User comments suggest confusion on item #4. If documents are specified by the customer why aren't they the same as items #1 and #2? J001 doesn't have an item #4.		
Staff	1.8		4.	User recommendation to add a row to Table 1-3 for "Marking"		Accepted to add this to both J001E & 610E referencing existing Note 2. <Feb07>
Jim Moffitt, Moffitt Consulting IPC Staff	1.x			The terms "are to be" and "need to be" and "must" may not have sufficient understanding by users. What if the user doesn't accomplish a "need to be" requirement?		J001 and 610 committee leaders will review all occurrences of these terms and provide recommendations to the committee <Feb07>
Mel Parrish, STI Electronics	1.x	T	5.	Neither 001 or 610 has a defect for components that are not installed/missing. It was in the previous MIL Specs as a defect code.		
Blen Talbot, L-3 Communications	4.2	T	6.	We need to consider moving the criteria from 620A, section 9.1.1 into the 610E. These jack posts are use on circuit boards. The 620A criteria is included in the draft at 4.2 to facilitate review.	(Staff recommendation to place in Clause 4.2)	
Mari Pääkkönen, Nokia Seppo Nuppola, Nokia	4.3.2.1		7.	Also 7.5.5 This comment deals with the requirements for component joints soldered with PIH (paste in hole) technique. X-ray and destructive tests can be used during solder joint qualification phase. These methods help for ensuring the capability of process. **Target Class 1, 2, 3** • The component and the solder joint areas must be thoroughly wetted. • Vertical fill is 100 % **Acceptable Class 1, 2, 3** • Evidence of wetting where the solder joint is visible (pin, barrel and annular ring) both side of the printed wiring board • Vertical fill ≥50 % **Defect Class 1, 2, 3** • No evidence of wetting	There are not any quality requirements for PIH connectors. The requirements for intrusive soldering (see Version D, page 7-50) can be used for PIH technology. The requirements for intrusive soldering are stricter than these new requirements.	

				• Vertical fill < 50 % <pictures provided>		
Staff	4.3.2		8.	This section seems to mix up "pins" and "lands." Should land damage be in Section 10? Fig 4-20 A1,2 has criteria specific to non-functional lands but no associated D1,2 criteria. No A1,2 or 3 criteria for functional land damage.		
Dr. Roberto Moretti, Consultant	4.4.1		9.	Note: "…lacing tape.." <change to> "...securing tape..."	The term "lacing" should be avoided in clause 4.4.1, since it has a different meaning in the Standard, as defined in 4.4.2.	
Dr. Roberto Moretti, Consultant	4.4.1		10.	Accept-Class1,2,3 first bullet "Lacing or tie wraps..." <change to> "Tie wraps/straps..." second bullet "Spot tie wraps..." <change to> "Spot tie wraps/straps..." fourth bullet "...to secure the lacing,..." <change to> "...to secure the tie wraps,..." Accept-Class1/Process Ind-Class 2/Defect-Class 3 "...under stress at the wrap." <change to> "..under stress at the tie wrap/strap." Defect-Class 1,2,3 first and second bullet/Fig.4-40 caption 2. "tie wrap" <change to> "tie wrap/strap"	In this section the Standard uses "tie wrap" in a generic sense to indicate any type of restraining device. The following sections 4.5.1 and 4.5.5 maintain more correctly the difference between tie wrap (i.e. tape, ribbon) and strap (i.e. small belt). Moreover the protrusion requirement is not applicable to tie wrap (too thin - see Fig. 4-35 and 4-37). Stress criteria are applicable to tie strap also. On Fig.4-40 caption 2.,"Lacing or "should be deleted.	
Leo Lambert, EPTAC	4.4.2.1		11.	Figure 4-45 does not address the tie wrap in the lower part of the illustration. Replace fig 4-45 with Fig 14-14 of IPC/WHMA-A-620 which addresses the tie wrap. Also add bullet to 4.4.2.1. Defect Class 1, 2, 3, ▪ Sharp edges that are a hazard to personnel or equipment (2) Change existing Bullet under Defect Class 1, 2, 3, From Broken lacing ends are not tied off using a square knot, surgeons knot or other approved knot (2). To • Broken lacing ends are not tied off using a square knot, surgeons knot or other approved knot (3).		
Bill Butman, EPTAC	4.4	E	12.	Within this section there are several instances where the use of terms is inconsistent. For example; the use of the terms, Spot Ties, Tie Wraps, and the term Restraining Devices are not consistently used but are used rather unpredictably.	My intent is to bring to the committee members the locations where I believe we should add some standardization. Thus, you may be confused by my inconstant use of replace "spot ties/tie wraps with restraining devices, and vice versa. My suggestion is to pick one set of terms and use them consistently where appropriate.	

Bill Butman, EPTAC	4.4.1	T	13.	Figure 4-35 Problem: Target condition not defined for knot.	Recommendation: See page 4-20; D-1,2,3 Recommend adding the following bullet; Spot Ties or Lacing must be secured with a square knot , surgeons knot or other approved knot.	
Bill Butman, EPTAC	4.4.1	T	14.	Figure 4-35 Problem: Target condition for the length of the cut end of the tie wrap not defined. Problem: Target condition for the "squareness" of the cut not defined.	Recommendation: Add a target condition: Define the target length of the cut length. See the Acceptable condition at Fig. 4-36.	
Bill Butman, EPTAC	4.4.1	T	15.	Fig 4-35 Problem: Target 1-2-3; shows spot ties but calls them "Restraining Devices?"	Recommend using the term "Spot Ties" as shown in the figure.	
Bill Butman, EPTAC	4.4.1	T	16.	Fig 4-36 Problem: Shows Tie Wraps but calls them Tie Wraps. Should the term "Restraining Devices" be used?	Strive for consistency	
Bill Butman, EPTAC	4.4.1	T	17.	Fig 3-37 Problem: Shows a break-out tied with spot ties and tie wraps. But the text uses the words "lacing or tie wraps. Should the call-out be: Lacing or tie wraps, note that spot ties are shown. Or use the more generic term "restraining devices"?	Strive for consistency	
Bill Butman: Assemtech Skills Training	4.4.1	T	18.	Fig. 4-37 A-1,2,3 1st bullet. Problem: "Lacing of tie wraps are placed on both sides of a wire breakout." The term "spot tie warps" is not defined.	Recommendation: Change "lacing" to: "spot ties" or "restraining devices," as shown.	
Bill Butman: Assemtech Skills Training	4.4.1	T	19.	Fig. 4-37 A-1,2,3 2nd bullet. Problem: "Spot tie wraps are neat and tight". The term "spot tie warps" is not defined.	Recommendation: Change "spot tie wraps" to: "spot ties" or "restraining devices," as shown.	
Bill Butman, EPTAC	4.4.1	T	20.	Fig 4-37 4th bullet Problem: . "-----approved knot is used to secure the lacing----"	Recommend: This term should be changed from "lacing" to: "spot ties" as shown.	
Bill Butman, EPTAC	4.4.1	T	21.	Fig. 4-39 Problem: This shows a Tie Wrap but calls out a "wrap." Should the text be,"wire is under stress at the restraining device. (No slack)".	Strive for consistency	
Bill Butman, EPTAC	4.4.1	T	22.	Fig 4-40 Problem: This shows spot ties and tie wraps, but calls out spot tie wraps.	Recommend the use of the words Spot Ties and Tie Wrap, or use the more generic term, "restraining device."	
Bill Butman, EPTAC	4.4.1	T	23.	Fig 4-40, D 1-2-3, fourth bullet: Problem: This figure needs to be clarified.	Recommend that the text add a reference to Fig. 4-41. Currently the reader must guess the reason for Fig 4-41. See Fig. 4-37, A 1-2-3, fourth bullet for an example of calling out a specific figure for the reference.	

Bill Butman, EPTAC	4.4.2	T	24.	TITLE: "Wire Bundle securing – Lacing." Within this General Section, the term "Cable Tie" is used. By my definition, a cable tie is also called a "tie wrap."	But, because this general section pertains only to lacing, and lacing is done with a cord or tape, I recommend that the term "Cable Tie" be stripped from this section. Replace the term "Cable Tie" with "Spot Ties or Lacing," as both use cord or tape. But if the distinguished committee members feel that the cable tie is not a plastic tie wrap, but is made using a cord or tape; then I recommend that the term Cable Tie be replaced with the term; "Cable Tie/Spot Tie".	
Bill Butman, EPTAC	4.4.2	T	25.	Problem: Within this section (pages 4-22, 4-23) the term "Restraining Devices" is used. By my definition, restraining devices can include plastic tie wraps. But because this section pertains only to lacing, and lacing is done with a cord or tape, I recommend that the term Restraining Device be stripped from this section. Replace the term Restraining Devices with "Lacing."	But because this section pertains only to lacing, and lacing is done with a cord or tape, I recommend that the term Restraining Device be stripped from this section. Replace the term Restraining Devices with	
Bill Butman, EPTAC	4.4.2	T	26.	General Information Problem: The term for the plastic restraining devices is not defined. Is it a Tie Wrap? Is the term defined in the IPC-T-50? Also not defined is the term "Lacing". (My copy of the T-50 is old.)	Recommend that in the general section for this paragraph the following be added. "Restraining Devices: May be plastic Tie Wraps (Zip-Ties) or spot ties or lacing using lacing tape."	
Bill Butman, EPTAC	4.4.2	T	27.	General Information Problem: "Lacing is a continuous lace." Lacing has closer spacing than cable ties. Criteria for cable ties apply to lacing. (Cable Ties? Are these tie wraps. Zip-Ties?) The term "Cable Ties" is used. What is the definition? Lacing differs from cable ties/tie wraps.	NOTE: This section applies only to lacing. . Recommendation: Cable tie requirements should not be addressed here. Some can state that this is only a comparison to the greater distance between (spacing) of individual "cable ties." However, I believe that a better comparison would be between the spacing of "lacing" and "spot ties." (Both lacing and spot ties are usually made with the same material, as apposed to the use of plastic cable ties.	
Bill Butman, EPTAC	4.4.2.1	T	28.	Fig 4-44. Target 1-2-3 2nd Bullet Problem: "Restraining Devices do not have sharp edges ----."	Recommendation: Delete this sentence. This section is titled: "Wire Bundle Securing – Lacing". Lacing, because it is not plastic, can not have sharp edges. And add an acceptable bullet to Page 4-19, figure 4.36 that states: "Tie wraps do not have sharp edges."	
Bill Butman, EPTAC	4.5	T	29.	General Information. Second Sentence. Problem: "Wire bundles are positioned ---. "	Recommend: "Wires within bundles or wire bundles are positioned ---." Wire crossover is more of a problem than bundle crossover.	
Bill Butman, EPTAC	4.5.1	T	30.	Fig 4-46, Target, second bullet; Problem: "---- with tie wraps/straps. "	Recommend removing the new term "straps" and keeping the term "tie wraps".	

Bill Butman, EPTAC	4.5.1	T	31.	Fig 4-47 Defect 3; Problem: "Wires --- a restraining device."	Recommend changing the term "restraining device" to tie wrap/spot tie.	
Bill Butman, EPTAC	4.5.3	T	32.	Fig 4-50 Defect 3, Problem: "Spot ties or tie wraps that ---."	Recommend changing the terms "spot ties or tie wraps" to "Restraining Device."	
Bill Butman, EPTAC	4.5.4	E	33.	Fig. 4-52, A 1-2-3, fourth bullet; Problem: "Sleeving extends on to the --- ".	Change "on to": to "onto".	
Bill Butman, EPTAC	4.5.5	T	34.	Fig 4-54; A1-2-3; Problem: "Spot ties or tie wraps/straps are placed near --- ".	Recommend changing the terms "spot ties or tie wraps/straps" to "Restraining Device."	
Bill Butman, EPTAC	4.5.5	T	35.	Fig. 4-54, D-3; Problem: "Spot ties or tie wraps/straps are placed over --- ".	Recommend removing the new term "straps" and keeping the term "tie wraps", or use the term "Restraining Devices".	
Bill Butman, EPTAC	4.5.5	T	36.	Fig 4-55; D1-2-3; Problem: "Spot tie or tie wrap is placing stress on the ---".	Recommend changing the terms "spot tie or tie wrap" to "Restraining Device."	
Staff	5.1		37.	Figure 5-13; replace next Rev. Looks too much like a fracture		Staff action to correct in 610E & J001E <Feb07>
Staff	5.2.10		38.	D1,2,3 reword bullet to the actual defect condition Suggested to delete D1,2,3 Add: Note: See 10.2.9.for criteria related to damage that may be caused by fillet lifting.	Causes shouldn't be defects. The downside of this note is that shrinkage that doesn't separate fillet to land but instead pulls the land off the board laminate isn't really fillet lifting.	
Bill Butman EPTEC	5.2.10	T	39.	Add: Acceptable – Class 1, to the condition described for the secondary side of the board. Currently the condition is listed as: PI – 2, D – 3.	The Acceptable – Class 1,2,3 covers the condition when fillet lifting occurs on the primary side of the board. The Acceptability for Class 1 is not listed when the condition occurs on the secondary side of the board. Get a picture showing the condition on the secondary side of the board. NOTE: if this is accepted, Test for MOD 4, Question 14 must be changed. Currently Question 14 does not have a correct choice. As the reader of the manual can infer that the stated condition is Acceptable for class 1.	
Pratap Singh	5.2.11		40.	What IPC has missed about Lead free solders is about time zero 'Shrinkage cavities' or shrinkage cracks. After inspecting 50 plus cards from different products and subjecting them to thermal cycles, it is observed that some of these shrinkage cavities/cracks grow resulting in solder joint failures. This seems to apply mostly to pin solder joints.		Staff to contact commenter for more info. High interest in these results but need more info. What solder, and what specifically are "pin solder joints" IPC Message to commenter 8/11/07

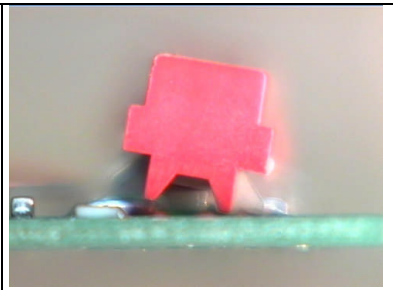
Werner Engelmaier, Engelmaier Associates, L.C.	5.2.11	T	41.	Discussion regarding hot tear from a msg exchange 3/24/07 The described issues—pad lifting, fillet lifting, fillet tearing [also called shrinkage fissures—are all caused by the same phenomenon. The combination of larger delta-T from solidification to RT, the higher strength of SAC-solders, faster cooling rates because of higher starting temperatures creating more cooling rate differences, more complex metallurgy, large differences in thermal mass, create stresses in the solder fillets that will cause the 'weakest link' to give. Sometimes the weakest link is the pad attachment to the resin matrix, in other cases the interfacial strength between IMC layers and Cu pad, in others the solder volume itself. Of course, none of these are pretty, but unfortunately, they are a characteristic of the LF-soldering realities. From a purely reliability point of view, none of these pose a mechanical reliability problem, even long-term. These 'defects' do not pose a real latent conditions in terms of loss of functionality. I am more concerned with the possibility of corrosive damage, particularly in the cases of pad lifting and fillet lifting, less so with fillet tearing, because of the exposed Cu. And I certainly would not make a differentiation between what is happening on the termination side vs. the component side as 610D does. That makes little reliability sense--if it is acceptable on one side, why not the other? That looks to me like simply calling it 'bad,' because on the termination side you can see it and it is hidden on the component side. As an example of a real reliability issue, I am much more concerned with accepting a 75% hole fill, because the stress concentration posed by the partial fill can cause plated-through hole Cu barrel failure. # # # # 2nd msg My comments regarding the effect on reliability rests on the general situation, where through-hole leads exert virtually no loading on the SJs during operation--there are, as almost always exceptions. I certainly have seen PTH-leads that cyclically loaded pins/SJs to failure. The maximum loading condition is typically along the leads or at most 45°away from the lead--thus, not really in line with the fractures. To your specific question. No, I do not see how to get rid of these 'defects.' One could try heat the whole assembly to a higher T prior to the wave and than cooling the whole assembly much slower, but that is likely to have more serious--in a real sense--consequences.		
Leo Lambert EPTAC	6.2.1		42.	Rolled flange: Separate Acceptable Class 1, 2, 3 second bullet to two bullets: Up to three radial splits or cracks separate by at least 90 degrees To • No more than 3 radial cracks • Radial cracks are separated by 90 degrees or more. Change Defect Class 1, 2, 3 fourth bullet to read from: • Splits or cracks that are not separated by more than 90 degrees To: • Radial cracks are separated by less than 90 degrees.	Clarity of words and easier to understand. This also helps the exam question by removing the ambiguity of positive and negative words within the same sentence.	

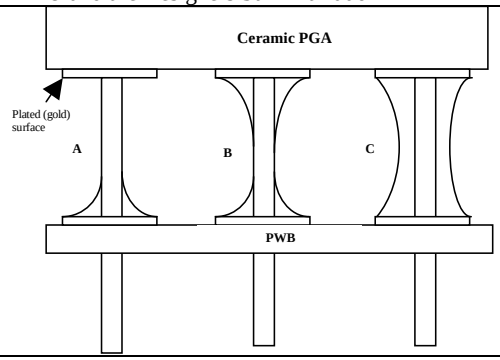
Leo Lambert, EPTAC	6.2.5	T	43.	Change title to add word, Flat Flange/ Fused in Place	Clarify since it only applies to flat flanges.	
Leo Lambert, EPTAC	6.3	T	44.	D 2,3 – Change criteria From: *Solder does not wet the tinned portion of the wire* to "Solder does not wet the surfaces of the wire strands to be tinned"	Clarify condition, to eliminate the confusion of the word tinning from a noun to a verb.	Committee did not accept this recommendation <Feb07>
Staff	6.6.2		45.	There is a conflict in 6.6.2 on page 6-16. The topic is stress relief bends in single wires attached to terminals. Next to Figure 6-31 and also next to Figure 7-9 on page 7-7 is the same criteria--A1, P2 D3 does not meet bend radius requirements of Table 7-1. However, next to Figure 6-32 it is a defect for all three classes if it does not meet the bend radius requirements of Table 7-1.	A1, P2, D3 twice, D1,2,3 once. Seems like A1, P2, D3 wins.	
Jim Moffitt, Moffitt Consulting Services	6.6.2	T	46.	I offer the following recommended revision to eliminate some of the ambiguity presently in Paragraph 6.6.2 on Pg. 6-16 of IPC-A-610D. The proposal is included in the Chapter 6 draft to facilitate committee review.		
Bill Butman, EPTAC	6.7.3	T	47.	Fig. 6-46, D 3. Problem: "Any straight through wire is not staked." This entry is in conflict with: Page 6-23, Fig. 6-47, D 1-2-3. "When required, the wire is not staked or component body not bonded to board or adjacent surface or retained by a mounting device." These words imply that there are times when a class 3 straight through wire may not require staking or bonding. (When required) Which conflict with the D3 statement that requires the staking of all class 3 straight through wires.	Recommend D1-2-3 be changed to D1-2 only. Therefore, class three must always be staked. (See page 6-20, Fig 6-40 A3.)	
Leo Lambert, EPTAC	6.7.6	T	48.	A,1 p2, d3 does not agree with J-STD-001, 5.4.4 001D wire wrap to hook shall be 180 °; A1D2,3; 001D 5.5 leads wrapped less than 180 ° shall have 100% wetting lead to terminal D1,2,3 610D 6.7.6 page 6-26 wire wrap to hook less than 180 ° A1P2D3, 6.10.5 page 6-47 less than 100% fillet with wrap is less than 180 ° D1,2,3 620A 4.8.5 page 4-28 wrap to hook less than 180 ° A1P2D3 but less than 90 D1,2; 4.9.5 page 4-39 less than 100% fillet with wrap is less than 180 ° D1,2,3	001 was changed to A1, D2, 3 and 610 was not	<90° D1,2,3 ≥90° <180° A1P2D3 <180° wrap <100% lead to terminal contact wetting D1,2,3 <Sep07> Staff has insufficient notes from the Feb meeting to resolve this

Bill Butman, EPTAC	6.7.8		49.	Fig 6-60, Target – 1-2-3, Second bullet: Problem: "Turrets – Wire contacts --- and wraps around or interweaves each terminal."	Recommend: Change to: "Turrets – Wire contacts --- and wraps around 360 degrees or interweaves each terminal." Adding the number of degrees eliminates any problems with what the writer means when stating, "wraps around". See third bullet for an excellent example of what I mean. Also see A1, PI 2, D3, first bullet.	
Bill Butman, EPTAC	6.7.9		50.	Fig 6-64 Problem; there is a conflict with this sentence and the next. This sentence states: "Wire has less than 180 degree wrap. This sentence states: "Wire has less than one wrap around terminal". NOTE: "Wire has less than one wrap around terminal". This can be any amount of wrap, from 1 degree up to 359 degrees. For the P2 condition, do we mean more than 180 but less than 360? If yes we should say so.		
Bill Butman, EPTAC	6.7.9		51.	Fig. 6-64 Change: Defect – Class 2 To: Defect – Class 1 - 2	I believe that this is an oversight on the part of the committee. We have not defined a Defect Condition for Class 1. I'm saying that for class 2, a wrap between 180 degrees and 359 degrees is a PI. While any wrap less than 180 degrees is a defect for class 1 and 2. And for class 1, any wrap greater than 180 degrees is acceptable. IF the committee meant that anything less than 180 degree wrap is also a Class 1 defect, then the change should be accepted.	
Committee Feb07	6.9	T	52.	Action Jim Moffitt, Moffitt Consulting Services and Sue Spath, Solectron, to review 6.9 and develop proposal for committee review. The proposed changes are included in the Chapter 6 draft to facilitate committee review.		This was completed Feb 07.
Dr. Roberto Moretti, Consultant	6.9.1		53.	Accept-Class1,2,3 first bullet "...spiral lay of the wire." <change to> "...spiral lay of the strands."		Accepted <Feb07>
Staff	6.9.2		54.	Placement - A1,2,3 first bullet and A1 P2 D3 Birdcaging does not exceed one strand diameter isn't in J001		Deferred to 001 committee; this is now an action on 001E comment list <Feb07>
Dr. Roberto Moretti, Consultant	6.9.3		55.	Target-Class 1,2,3 "Wires are not scraped…." <change to> "Wire strands are not scraped...."	Staff comment: strand/wire/lead/conductor damage could be better addressed and perhaps consolidated here. This clause is called "Conductor Damage" so perhaps the best term would be "Conductors are note scraped…"	

Leo Lambert, EPTAC	6.10	T	56.	D 1, 2 & D 3 - add to end of sentence "of diameter of wire" To clarify and answer the question of % of what.	Clarify condition	
Leo Lambert, EPTAC	6.10.1	T	57.	A 1,2,3 Last bullet, should be changed to the following: defect Class 3, and P2 due to requirement 6.7.1 Wire Placement, Add Process Indicator Class 2 To: Solder is wetted to 100% of contact areas between the wire/lead and terminal interface for leads wrapped between 90 and 180 degrees. Add: Defect Class 3 Solder is wetted to 100% of contact areas between the wire/lead and terminal interface for leads wrapped less than 180 degrees. Wire placement 6.7.1 drives this requirement	To make sections of text agree and clarify the conditions to the users.	
Leo Lambert, EPTAC	6.10.2		58.	Last two bullets on Defect Class 1, 2, 3, should be moved next to figure 6-95 and 6-96 as they reference wrapping of the wire as opposed to going straight between the tines of the terminal .	The location of the defects conditions are in wrong location for understanding of defect.	
Leo Lambert, EPTAC	6.10.5		59.	Change title from Terminals – Solder – Hook/ Pin To: Terminals – Solder - Hook	Hooks are round and not square. Square Pins criteria is not an applicable conditions in this case and should be handled separately. To eliminate confusion and make the page clearer. Staff comment: 6.7.1 is placement on turrets/straight pins; 6.7.6 is placement on hooks; 6.10.1 is solder only to turrets, 6.10.5 is solder to hooks/pins. Perhaps pins should be separated to their own clause OR always use the term "round pins" so there is no confusion to square pins.	
Leo Lambert, EPTAC	6.10.5		60.	Second bullet **A, 1, 2, 3** is called out as **P 2, A,1** per 6.7.6 Wire placement. This creates a discrepancy between assembly criteria and soldering criteria. Change Acceptable Class 1, 2, 3, Bullet two *Solder is wetted to 100% of the contact area between the wire/lead and terminal interface for leads wrapped less than 180 degrees.* *To* Process Indicator Class 2*: Solder is wetted to 100% of the contact area between the wire/lead and terminal interface for leads wrapped less than 180 degrees.*	6.7.6, calls for wire placement on Hook Terminal. This creates consistency in the document	
Staff	6.11		61.	Post-solder - A1,2,3 first bullet and A1 P2 D3 Birdcaging does not exceed one strand diameter isn't in J001		Deferred to 001 committee; this is now an action on 001E comment list <Feb07>

Dr. Roberto Moretti, Consultant	7.1.2.1		62.	Accept-Class 1,2,3 first bullet "Leads for through-hole mounting extend at least..." <change to> "Leads of through-hole mounting component extend at least."	Criteria for lead bend are applicable also when component is not through-hole mounted (see 6.4 Fig.6-21, 6.7 Fig.6-34 etc) Hence "for "should be changed to "of" to indicate the type of component and not the type of mounting. For the same reason "through-hole mounted component" should be changed to "through-hole mounting component"(see below).	
Dr. Roberto Moretti, Consultant	7.1.2.1		63.	Accept-Class1/Process Ind-Class 2/Defect-Class 3 "Lead bend of through-hole mounted component is less..." <change to> "Leads of through-hole mounting component extend less..."	It's not the "lead bend" but "lead extension" which is less than... (see page 7-6 Accept-Class 1,2,3 first bullet).	
Staff	7.1.2.1		64.	Conflict with J001D. 610 states one lead D or 0.8 mm whichever is less, but J001 states "shall not be less than 0.8 mm"		Accepted to Modify 001 to match 610 <Feb07>
Staff	7.1.2.1		65.	Conflict with J001D. 610 states one lead D or 0.8 mm whichever is less, but J001 states "shall not be less than 0.8 mm"	<Sep07> revisit after I found some more notes. The requirement for "whichever is less" means that the minimum spacing to start of the bend, even in thick leads, only has to be 0.8 mm from the body BUT leads less than 0.8 mm D could start the bend even closer. Both 610 and 001 need to address this. Leo Lambert, EPTAC comments: It seems to me that there are two criteria of which we are talking about, one the lead bend radius, and two, where the lead bend radius should be. From 610, Fig 7-8, A1, 2, 3, Leads … extend at least one lead diameter or thickness but not less than 0.8mm from the body. This is a distance criterion from the component body. From 610 Fig 7-11, A1, P2, D3, Lead bend … is less than one lead diameter or 0.8mm, whichever is less, is also a distance criterion. Why don't we just say it that way? If you want to use the same verbiage with some modification, you could also have it read as follows. The distance of the lead bend radius of through-hole mounted components is less than one lead diameter or 0.8mm from the component body, solder bead or component body lead seal. Change bullet next to Fig 7-11 to read: Lead bend of through-hole mounted component is less than one lead diameter or 0.8 mm [.31"], whichever is less. By removing the words … from the component body, solder bead or component body of lead seal, makes the statement more definitive. By doing this you also meet the requirements of J-STD-001, where a lead shall extend from the body at lead one lead diameter or thickness but not less than 0.8 mm before the start of the bend radius. The bend radius is another requirement and is identified in table 7-1 and it is based upon lead sizes.	

Prapot A, Sanmina-SCI Thailand	7.1.8		66.	We have found the SMD connector have been tilted after placed to the boards. (See the attached photo for more clarification). The attached photo is looking at a short side. I did some rough measurements and I get a difference between the height of the two outermost corners on the short side of about 0.9mm. With a connector this small, that means there is a fairly large amount of tilt in degrees and it is very noticeable. I have checked with the IPC-A-610 rev.D regarding the SMD connector tilted but there is no criteria established for this case. It has only PTH connector criteria.		Action Greg Hurst BAE SYSTEMS to develop criteria for surface mount connectors for both 001E and 610E <Feb07>
Staff	7.4		67.	Intro para needs correction; for unsupported holes, straight through is acceptable only for Classes 1,2. Class 3 must be clinched.		
Bill Butman EPTAC	7.4.1	T	68.	Under the Target Condition: Add the requirement that a Clinch is required for Class 3	Although Figure 7-69, Note 2 states: "Clinch required for Class 3." I consider this to be part of the "Figure." Figure 7-69, Note 1 states: "No Plating in barrel." This is informative, telling the reader what an "Unsupported hole" is. (This is part of the figure information, not a requirement.) I don't think that the committee meant for note 2 to be informative. The clinch for class 3 is a requirement, and should be listed with the other bulleted requirements.	
Bill Butman EPTAC	7.4.1	T	69.	Add a defect requirement for a component that is required to be mounted off the board. The defect is when the height is too great and violates the maximum height limit of the assembly. "Component height exceeds user-determined dimension (H)."	Currently there isn't a height limit established for Unsupported Holes – Axial Leads – Horizontal. See: 7.5.1, Defect – Class 1, 2, 3 for an example of the same requirement for Supported holes.	
Staff	7.4.3		70.	User questions why 7.4.3 unsupported hole protrusion has a Target but 7.5.3 support hole protrusion does not		
Aimee Siegler, Benchmark Electronics	7.5.1	E	71.	Defect Class 3 and Figure 7-92. The distance between the component body and the board is larger than 1.5 mm [0.059 in].	If this is meant to refer to clearance, should reference (C) since the word distance has been used for (D). Either way, please provide ref to C or D for clarification for next Rev.	Action Tino Gonzalez, ACME Training and Consulting, to propose clarification to 610E and 001E
Mark Logterman, Cisco	7.5.5		72.	This proposal is for class 2 only. Change the minimum acceptable solder condition for "vertical fill of solder" from 75% of PCB thickness to a	Cisco studies and other industry reliability studies* have shown PTH solder joint reliability to be a function of the vertical length of the solder which has wetted to the pin within the barrel of the PCB thru-hole regardless of PCB thickness.	Action Mark Logterman, Cisco, Elizabeth Benedetto, HP and Mel Parrish, STI action to develop proposed

				minimum pin wetted length (regardless of PCB thickness). NOTE: Minimum Pin wetted length would be a static number (say .030"; for example purposes **only**). For inspection purposes, a table or chart could be provided indicating what percent the minimum pin wetted length needs to be for various PCB thickness ranges.	Increased PCB thickness and layer counts, use of less aggressive fluxes for environmental reasons, and implementation of Pb free solders have all contributed to extreme difficulty in complying to the current IPC requirements on PCBAs with .092" thickness and above with multiple power/ground planes. The proposal being submitted is a very general statement intended only to get the topic on the table as revision E activity begins. Cisco will provide reliability test data as required to support discussion and development of detailed specifications. The intention is that other participating companies will provide data as well. *- i.e., Ernesto Ferrer, Elizabeth Benedetto, Gary Freedman, Francois Billaut, Helen Holder, Hewlett-Packard Development Company, L.P. "Reliability of Partially Filled SAC305 Through-Hole Joints", IPC Printed Circuits Expo®, APEX® and the Designers Summit 2006	hole fill criteria
John Mastorides	7.5.5		73.	Illustration proposal for pin grid array solder requirements		
Joe Kane, BAE SYSTEMS	7.5.5.10		74.	Also 001 6.1.5 610D says that there is no defect condition for an unfilled hole if it doesn't wet properly. J-1D Paragraph 6.1.5 says that holes may be left unfilled, if wave soldered and masked, but doesn't really say what is acceptable if the hole is not masked but just doesn't fill. We know that the intent is that the hole may be left unfilled, but what if we wave solder, don't mask, but there is poor wetting inside the unfilled hole? A hard horse might say that in this case the requirements of 6.3.2 apply, including wetting and 25% hole recession. J001D 6.1.5 has the same criteria as 610D. No SHALL words so not requirements to be filled. When Rev D was being developed, no one on the committee could provide any support for the Rev C requirements to meet Figure 9-2, so the figure and requirement to meet the figure were deleted from Rev D. J001D Clause 1.13.2 will need to	I believe there are specific exemptions that are unnecessarily restrictive. PTH's may be left unfilled if: 1. They are not subjected to a wave soldering operation. 2. There is a wave solder operation but the holes are masked. It doesn't say what happens if I wave solder, don't mask, and the hole doesn't fill, or partially fills. I just don't see why there's a distinction between mass and hand soldering. I also think the first sentence is a little confusing about unsupported holes - is it all unsupported holes with leads, or those with leads that are not mass soldered? And why is it just unsupported holes with leads? Suggest that 6.1.5 could be simplified like this:	

				apply now. J001 6.3.2 specifically is titled "Through-Hole Component Lead Soldering". Someone can be as hard as they want, but if there is no lead this criteria is not applicable.	"PTH's used for interfacial connections and unsupported holes need not be filled with solder."	
Staff	7.5.5.6		75.	Need to separate solder in lead bend and solder touching component body issues for through-hole terminations. What about solder NOT in the lead bend but still in contact with component body, e.g. DIPs		
Mari Pääkkönen, Nokia	8.2.2.6		76.	Acceptable –Class 1,2,3 • Wetting is evident (fig. x), lead-free soldering.	Coils with Ag/Pd coated terminals in lead-free process. Abnormal shape of fillet, solder near the terminations of the component No reliability risk	
Dr. Roberto Moretti, Consultant	8.2.2.9.3		77.	Accept-Class1,2,3 and Defect-Class1,2,3 second bullet "All components..." <clarification>	"All" adjective is confusing. If it refers only to stacked parts, the verbiage "Stacked components(or parts)..." is more clear. Maybe Defect second bullet is wrong, since to have a defect is not necessary that "All components do not meet..." but is sufficient that one component at least does not meet.	
Dr. Roberto Moretti, Consultant	8.2.5.4		78.	Target-Class 1,2,3 "…along full length of lead." <change to> "…along full length of the lead foot."		
Dr. Roberto Moretti, Consultant	8.2.5.4		79.	Accept Class 2,3 first bullet and Defect Class 2,3 first bullet "...foot length (L) is greater than three (W)..." <change to> "...foot length (L) is greater than or equal to three (W)..."	To match with Table 8-5.	
Staff	8.2.5.8		80.	Also refer to 8.2.6.9 and 8.2.7.8 All of these refer to connection issues because of a lead being out of alignment but the wording is different. I suggest that 8.2.5.8 says it best—focusing the defect on the end solder connection. The other two establish the defect "lead not touching the land." After soldering if the connection is good it doesn't matter if the lead was touching the land and often they aren't—there's Dim. G between bottom of lead and top of land.	Suggest further wordsmithing to be used in all three places: D,1,2,3 Any component lead alignment, coplanarity, or damage that prevents formation of an acceptable soldered connection.	
Staff	8.2.6		81.	Table 8-6 Dim A 50%/25% (W) or 0.5 mm whichever is less; 8.2.6.1 A1,2 and A3 no reference to 0.5 mm is a conflict		

Bill Butman, EPTAC	8.2.6.8	T	82.	Figure 8-103, Illustration for "Round Leads." Change the "W" dimension, To "T".	To my knowledge this is the only lead type that has a Side Joint, "Height" requirement. Table 8-6, DIM Q states that this Dimension is: , (G) + 50% (T). But figure 8-103 for round leads calls this dimension "W". There is a conflict between Table 8-6 and Fig. 8-103. I believe in every case when stating the dimension for SMT leaded devices, the letter "T" is used to indicate this dimension. I agree that when discussing round leads, dimension, "W" and "T" would be the same. After all we are talking about a diameter. However, to maintain some consistency in referring to the "height" of a lead, we should use the letter "T".	
Staff	8.2.7		83.	Table 8-7 Dim F Class 1 conflicts with J001D Table 7-9	J001D Dim F Class 1 is Note 3; Wetting is evident.	
Dr. Roberto Moretti, Consultant	8.2.7.6		84.	Accept Class 1,2 "Heel fillet heigth (F) is minimum 50% lead thickness (T) plus solder thickness (G)." <change to> "Heel fillet heigth (F) is minimum solder thickness (G) plus 50% lead thickness (T)."	To avoid the interpretation 50% (T+G) and to match with Table 8-7 and all other similar clauses in section 8.2.	
Dr. Roberto Moretti, Consultant	8.2.8.3		85.	Target-Class 1,2 "End joint width (C) is greater than land width (W)" <clarification>	Since C is measured in the narrowest point of the joint, can C be greater than W?.	
Staff	8.2.8.4		86.	Figure 8-130 D is only as wide as the lead, not the land		
Christopher Sattler, AQS - All Quality & Services, Inc.	8.2.x	T	87.	<Deferred from Rev D development> Add LCC with J leads added Suggested criteria and some illustrations have been placed in the draft following 8.2.7 to facilitate committee review.		
Christopher Sattler, AQS - All Quality & Services, Inc.	8.2.x	T	88.	<Deferred from Rev D development> Ceramic BGA criteria and some illustrations have been placed in the draft following 8.2.12 to facilitate committee review.		
Klaus-D. Rudolph , Siemens ICN Christopher Sattler, AQS - All Quality & Services, Inc.	8.2.12	T	89.	<Deferred from Rev D development> Add a new Chapter for Column Grid Array: Column grid array criteria and some illustrations have been placed in the draft following 8.2.12 to facilitate committee review.	Missing in Revision D	
Dr. Roberto Moretti, Consultant	8.2.13		90.	Table 8-13 Note 5 <change to > Note 5 from IPC-001D Table 7-15	This note is more clear and defines the dimension H.	
Committee meeting Feb07	8.2.14	T	91.	During the meeting there was discussion about side overhang of D-Pak components. Jennifer Day, Sanmina-SCI agreed to contact Ron McIlnay, American General Contracting & Consulting because he had presented some of the original criteria. His comments: Comment 1: The issue with D-pak's is that they are made for high power or energy switching that endure instant high current short circuit conditions. In most cases, the assemblers don't have a clue as to what the working and surge currents are with the design. Every D-pak manufacturer that I am aware of calculates the energy capability (including margin) based on having "total" foot contact to the mounting pad. Therefore, if the design did not account for 50% derating (very few designs are derated properly), then the soldered joint (and not the lead) will take the brunt of the energy shock, and that is a		

				recipe for disaster as the constant heating/cooling will cause grain boundaries, embrittlement and eventual failure. I suggested that if the design engineers did feel that their design can tolerate greater than 25% overhang, then they should "trump" that part of A-610 and add a note to their drawing allowing that condition. However, I don't think many engineers will want to hear that even 25% of the foot area is going to be allowed to "hang over" on their product. Power Starvations does weird things to their logic circuitry also so they want to know that the soldered joint can handle more the twice the lead capacity. They never design for and worse yet, never test for "worst case" so they then get into these power starvations conditions the can be similar to "brown-outs. Comment 2: The company I was working for (Medtronic, Physio Control) had serious problems with "D-paks" off their pads as the product was external heart defibrillators. A massive amount of high voltage is stored a very large special capacitor, then converted into high current energy necessary to restart the heart and deliver that energy in a specific waveform. Because D-paks (FET's) act very well as high energy switches and can handling an enormous amount of high energy, they are the chosen component in designs needing that capability. In defibrillators, the high energy (over 400 joules) must have an absolute "best condition" mounting otherwise they won't be able to handle the massive amount of electrical current. When that happens, they fracture the soldered joints, then generally arc within the unit, rendering it inoperable …(not a good thing when someone is having a heart attack or has stopped all-together). D-paks (FET's) are also favorite components used in power supplies (tons of these always being produced), X-Ray, high speed wave-guide, radar systems and any system requiring high energy. My position on making D-paks requiring "tighter control" is because the engineers know what they need for the high power circuits, but assemblers don't. So it has been my position since the D-pak (FET's) are almost always used, and only used, in high energy circuits, then they should always be required to meet the tighter controls. Otherwise, companies will always be having troubles with "standards" and have to always be adding those conditions to their drawings and usually after they have experienced massive failures.		
Kelin Lim, NERA Electronics	8.2.x		92.	Need criteria for new connector termination type some illustrations have been placed in the draft following 8.2.14 to facilitate committee review.			
Steve Wall, Tiscali.CO.UK	9		93.	Need guidance regarding some component damage acceptance criteria from within EIA595 vs IPC-A-610. We have recently noticed some surface damage to some surface-mount 1208 capacitors on our PWBs from our sub-contractor which do not meet the requirements of IPC-A-610 (no damage allowed for class 3 products). From pursuing this back through our PWB sub-contractor, they have advised us that the parts are not being damaged through their process (tests have proven this) but the parts are being received by them in this condition. The component manufacturer release the parts to EIA595 standards which does allow surface damage.	We have, to date, no experience of electrical failure of these capacitors, the issue is only of a difference of acceptability between the IPC standard and the EIA standard. The component supplier has advised that they can supply components which will meet the IPC class 3 standards, but this will require an increase of 25% in the cost of the parts. From review of the component manufacturing process, a visual inspection is carried on the parts prior to electrical testing and any components that fail the EIA specification are rejected at that stage. My concerns are; 1. What are the reliability implications of using components which show minor surface damage which are within EIA595 standards but do not meet IPC-A-610 class 3 standards. 2. Which standard normally takes precedence.	

Staff	9.1		94.	A1,2,3 first bullet D1,2,3 first two bullets change "leaching" to "metallization loss"	Leaching is the process, metal loss is the defect	
Staff	9.3		95.	Missed when errata corrections were made; P2D3, defect is when chipouts DO enter the lead or lid seals, not when they DO NOT		
Joe Kane, BAE SYSTEMS	9.3		96.	says that "minor...chips" are acceptable for all 3 classes. This is consistent with J-STD-001D para. 3.9.6. On the next page, it says "Defect - Class 3" for chipouts on edges of **ceramic** components, even if they do not enter lead or lid seals or extend out into cracks. It's not clear if Figure 9-11 is a plastic or a ceramic part, but if it's ceramic, that cracked corner might be on the ragged edge of acceptability for cosmetic reasons, but we would be hard pressed to reject it per J-STD-001 3.9.6. Figure 9-14 on page 9-6 seems to show the real defects, and we suggest that on page 9-5, "Defect - Class 3" is in error, and this should be a PI for Classes 2 and 3.		
Joe Kane, BAE SYSTEMS	9.3		97.	(quibble) Figure 9-12 is referenced as a plastic part in the first bullet at the top of page 9-5, but some of us think that the part looks like glass.		
Staff	9.4	E	98.	D1,2 next to Figure 9-23 Recommend delete 3rd bullet "Any chip-outs in resistive elements.	1. This is already covered in 9.2 Chip Resistor Element 2. 9.4 is applicable to other kinds of chip components in addition to resistors. The criteria should be generic and not to a component function.	
Mari Pääkkönen, Nokia	9.4		99.	Section 9 Component Damage Acceptable –Class 1,2,3 • Component darkening in lead-free process. The degree of darkening varies according to the size of component. The smaller chips darken more.	Component darkening in lead-free process, especially in first-pass side after the second reflow. Reason for this phenomenon is the fact, that flux medium migrate into the surface of the metallization. Darkening is caused by atmospheric oxidation. Darkening is only cosmetic phenomenon and it has no effect on reliability.	
Joe Kane, BAE SYSTEMS	9.4		100.	Paragraph 9.4, at the top of page 9-9 has a defect for any chipout or nick on a chip component. This also conflicts with J-1 para. 3.9.6, and 610 para. 9.2, which allows chipouts in the top surface adhesive coating on chip resistors. Is the intent here that a minor chipout is OK for a resistor, but not for a capacitor or MELF? Or is the definition in J-1 better, and it's only a defect if it affects active elements like termination areas (endcaps)?		
Joe Kane, BAE SYSTEMS	9.4		101.	(quibble) The nick in Figure 9-27 is almost invisible on the page, much less out in the shop under 4x. Figure 9-28 doesn't look like a nick, crack, or chipout, but a loss of metallization, and might belong in 9.1. It looks like that's a blob of non-wetting solder on top, not a chipout.		IPC Action to make the nick more evident for next publication. <Sep07>
Staff	9.5		102.	Connector burrs stated for A1,2, not addressed for 3. "A3 no cracks" missing defect		
Many	10.2		103.	Measles differences against bare board standards		

John Mastorides, Honeywell Aerospace	10.2.4		104.	Provided several pictures to help show the criteria. The pictures are in 10.2.4 of the draft to facilitate committee review.		
Leo Lambert, EPTCAC	10.2.4	T	105.	Remove the word unaffected from the 2nd sentence of the defect criteria.	There is no definition of the word "unaffected" in either the acceptable condition of 610 and in 6012 B. The criteria calls for dimensional measurements and when the word unaffected is used the dimensions are to be measured from this unaffected area. If the condition does exist it is an affected area and the condition needs to be addressed be it either as acceptable or defective.	
Staff	10.2.7	E	106.	Add additional narrative to reinforce that post assembly bow and twist (**NO DEFECT**) is different from bare board criteria with defined limits.	Too many questions from users that just don't understand "should" and "end use."	
Mari Pääkkönen, Nokia	10.2.8		107.	New figures Proposed illustrations were placed in the draft at 10.2.8 to facilitate committee review.		
Susan (Mansilla) Hott, Robisan Labs	10.2.x		108.	Add Defect for cut/scored laminate surface	I would think the cut laminate would be a defect. Board Fabricators can't sell a board with cut laminate, why in the world could we accept cut laminate as a result of repair/rework or assembly process.	
Dr. Roberto Moretti, Consultant	10.2.8.4		109.	Accept Class 1 second bullet "....does not bend or flex transition area." <change to> "..does not extend into the bend or flex transition area."		
Dr. Roberto Moretti, Consultant	10.2.9.1		110.	Defect Class 2,3 second bullet "Reduction in width or length..." <change to> "Reduction in minimum width or length..."		
Joe Kane, BAE SYSTEMS	10.2.9.2		111.	We're puzzled by the defect condition in 10.2.9.2 on page 10-23, "Any lifting of a land if there is a via in the land". This seems to conflict with other parts of this clause, like Figure 10-39, which shows lifting less than the pad thickness on the same type of connection, but defines this as a process indicator. There's also J-STD-001D para. 9.1.4, which does not talk about this special condition.	We think that the intent might be to prohibit lifting for a filled via, i.e. a surface mount via-in-pad, but the implication here is that any unfilled PTH pad cannot be lifted to any degree. This seems unnecessarily restrictive. This defect should either be removed, or maybe changed to state: "Any lifting of a land if there is a filled via in the land." And if this is correct, the requirement should be added to J-1.	
Joe Kane, BAE SYSTEMS	10.2.9.3		112.	There's also the defect condition in 10.2.9.3, which must have been added in Rev. D, but I don't remember why or by whom. We think there should at least be a clarification of what is meant by "mechanical damage", because most any scratch or ding in an outer conductor will be caused by some sort of mechanical action. And note that J001 para. 9.1.5 doesn't make any distinction about how damage is induced, it just talks about the end result, i.e. the reduction in the conductor width or thickness.	Figure 10-43 doesn't do much to clarify this, because we don't think that it shows anything that clearly affects form/fit/function. Some of our sites put threaded hardware through plated features like the one in this picture, and a few dings on the edge are inevitable and mostly acceptable.	

Staff	10.3	T	113.	620A has an intro sentence in the clause for every kind of marking: "These criteria are applicable when content marking is required." Adding this to each kind of marking in 610E will clarify that 610 doesn't establish when marking is required.		
Dr. Roberto Moretti, Consultant	10.3		114.	Last but two sentence, second row "However,..., it is an acceptable condition if these markings are removed..." <change to> "However,..., it is an acceptable condition if these markings are not removed..."		
Dr. Roberto Moretti, Consultant	10.3.2		115.	Target-Class 1,2,3 last bullet "...no closer than tangent to a land." <change to> "...no closer than tangent to a solderable land."		
Dr. Roberto Moretti, Consultant	10.5.1.2		116.	Defect-Class 1,2,3 first bullet "...bridge adjacent noncommon circuits." <change to> "...bridge adjacent noncommon conductors."		
Leo Lambert, EPTAC	10.5.1.2	T	117.	Note adjacent to Fig 10-84 conflicts with Process Indicator for Class 2, 3 adjacent to Fig 10-85 The note was not in Rev C of the document and cannot find anywhere in my notes as to where it came from, recommend removing the note from this section or change it to the read as follows Blisters, scratches, voids that expose the laminate are acceptable as long as they don't bridge adjacent circuitry. I also recommend changing the Process Indicator Class 2, 3 on page 10-47 to read as follows Blisters/flaking which exposed base conductor material.	This needs a better explanation as it allows it on one side and defines it as a Process Indicator on the next page	
John Boyko BAE SYSTEMS	10.5.2.2		118.	A1,2,3 The coating may exhibit dewetting, ripples, fisheyes, or orange peel D1,2,3 Any voids(caused by), bubbles, adhesion loss (mealing) dewetting, ripples, fisheyes, orange peel, or foreign material that expose circuitry, bridge lands or adjacent conductive surfaces	Please look at defect conditions. I believe here is contradiction to the accept criteria. Fisheyes or orange peel (this one needs clarification especially since orange peel is a surface condition that could extend over a wide area. Is it possible that fish eye should be treated separate from orange peel?	
Staff	10.5.2.2		119.	clarification of Conformal Coverage A1,2,3 Fourth bullet should start "Voids do not bridge…" and D1,2,3 "Any voids that bridge…" Last bullet "coating is thin but still coats edges…" could be reworded for clarity. Some users require explanation of "thin on edges" vs Table 10-1 thickness measurement on flat, unencumbered cured surface…		

Staff	11.1	E	120.	Staff recommends extracting Solderless Wire Wrap criteria from 610E (and future 620B) and publishing this criteria in a separate document as a "Free Download." IPC is not opposed to naming/numbering it in a manner that retains a relationship to 610 and 620 for users that already have this identified on drawings/procurement documents.		
Dr. Roberto Moretti, Consultant	11.1.3		121.	Accept-Class 2 second bullet "End tail does not extends more than 3 mm from outer surface of wrap." Accept-Class 3 first bullet "End tail projects no more than one wire diameter from outer surface of wrap." Accept-Class 1 Defect-Class 2,3 "End tail is greater than 3 mm." Defect-Class 3 "End tail is greater than one wire diameter." <clarification>	It's not clear if requirements refer to two different characteristics i.e. the extension (length) and the projection (protusion) of the end tail or the two verbs are used as synonymous. "End tail is greater than..."should be changed to "End tail extension (projection) is greater than...."	
Dr. Roberto Moretti, Consultant	11.1.9		122.	Accept-Class 1,2,3 last bullet "Cut or fraying on the wrap" <change to> "Cut or frayed insulation"	To match with Fig.11-21 caption 3. If "wrap" is considered to be an appropriate word, here it indicates the insulation, See the clarification request on page 12-6.	
Dr. Roberto Moretti, Consultant	11.1.9		123.	Defect-Class 2,3 first bullet and Fig.11-23 caption 2. "...between wrap terminals" <clarification>		
Staff	11.2.2		124.	Wire routing; delete references to primary and secondary sides; not applicable to boards with components on both sides that are common now		
Staff`	11.2.4.1	E	125.	Title—"PTH/Via" perhaps should be just PTH. Vias really are not intended (per PCB acceptance criteria) to have leads in them and it could be introducing an unexpected failure mechanism.		
Staff	11.2.4.2	E	126.	Figure 11-36 is pretty poor in what it shows and how it doesn't show it very well. We could use some real pictures for all the jumper wires.		
Dr. Roberto Moretti, Consultant	11.2.4.3		127.	Accept-Class 1,2,3 and Defect-Class 1,2,3 first bullet "...(L)(from edge of land to knee of lead)." <clarification>	Requirement is clear but, for completeness, (L) should be re- ferred to a figure, as shown in Fig.11-44 for gull wing and Fig.11-48 for J leads . We note that Fig.11-38 and 11-41 do not pertain to this section (PTH). In fact Fig.11-38 is iden- tical with Fig.11-45 in SMT section.	
Staff	11.2.4.3		128.	Fig 11-38 wrong pix, this is PTH section		
Staff	11.2.4.3		129.	User questions why lead extending past knee is Defect for SMT 11.2.5.2 & 11.2.5.3 but not for PTH		
Leo Lambert, EPTAC	11.2.5	E	130.	Begin page with sentence "For all…." Move first two sentence to section 11.2.3 Jumper wires – Wire Staking	Not pertinent to section 11.2.5 Jumper wires, - SMT	
Dr. Roberto Moretti, Consultant	11.2.5.1		131.	Target-Class 1,2,3 second bullet "Solder fillet...." Accept-Class 1,2,3 "...solder connection..." both <change to> "solder connection length"	To comply with the more precise verbiage used in Defect-Class1,2,3 same page.	

Joe Kane, BAE SYSTEMS	11.2.5.4		132.	Para. 11.2.5.4 requires that the wire must make contact with half of the longest dimension of the land. Looks like this requirement was added in Rev. C, and we're not sure why. For a long pad, this could result in a pretty long contact length, which makes for a tough job of hand soldering, but doesn't add anything to the reliability of the connection. The old requirement out of MIL-P/C-28809 was that the contact length must be at least twice the wire diameter, which is similar to the way component lead contact is specified, and seems to make more sense:		
Dr. Roberto Moretti, Consultant	11.3		133.	Accept-Class 1,2,3 first bullet “Wires exiting connector are positioned as they would be at installation.” <clarification>	Clause means simply that wires are positioned correctly?	
Dr. Roberto Moretti, Consultant	12.2.1		134.	Accept-Class 1,2,3 first bullet “...follows the contour of wire wrap....” <clarification>	Since with solder cups we have no “wire wrap” in the usual sense, i.e. turns (Sec. 11.1 2nd sentence) or hooks (Sec. 6.7.1) around the terminal, either there is an error in the text or “wire wrap” here indicates the boundary surface of the wire conductor. In the latter case, the same expression has more than one meaning in the same argument of the standard and this should be avoided.	